APPLICATION		REVISIONS			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	A590	1	ADVANCE ENGINEERING RELEASE	5-6-88	[illegible]
		A	SPECIFICATION RELEASE	11/4/88	[illegible]
		B	REVISED PER ECO 890001	1-27-89	RMB

1.0 Description

This part describes the programming for a 16L8A PAL for the A500 PCB. The following equation is to be programmed into Commodore Part Number 390071-02. This programmed part becomes Commodore Part Number 390333-03. This PAL is used to generate memory timing for the A590 scsi.

COMMODORE PART #	STATUS				
390333-01	INACTIVE				
390333-02	INACTIVE				
390333-03	ACTIVE				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/-.02
3 PLACE DECIMALS +/- .010

DRWN C. Bonsall	4·26·88	commodore
SYSTEMS ENG		
TEST ENG		
CIRCUIT ENG		
COMP ENG		

TITLE
IC, PAL, 16L8A, Programmed
Memtiming

SIZE	DRAWING NO.
A	390333

SCALE none | SHEET 1 OF 3

```
/** PAL used to generate RAS and CAS for scsi expansion board for A500 **/
/** 8/24/88 105 ns _AS margin (newmem4 simulations).  All timing
        margins checked  **/
/** Newmem5 actually.  This is the one that is like newmem4 but has a
        slightly extended mux signal to avoid a possible race **/
/** Newmem7 is like newmem5, except it has _DTACK extended until _RAMSEL
        goes away **/

PARTNO          16L8A;
NAME            u5nm7;
DATE            8/24/88;
REV             01;
DESIGNER        augenbraun;
COMPANY         commodore;
ASSEMBLY        XXXXXXX;
LOCATION        wchest;

/**     Inputs          **/

PIN 1           = !7m;
PIN 2           = !c3;   * CCKQ
PIN 3           = cdac;
PIN 4           = !c1;   * CCK
PIN 5           = !ram_sel;
PIN 6           = a17;
PIN 7           = a18;
PIN 8           = a19;
PIN 9           = a20;
PIN 11          = DUMB;


/**     Outputs         **/

PIN 12          = a17muxa18;
PIN 13          = mux;
PIN 14          = !cas0;
PIN 15          = !cas1;
PIN 16          = !cas2;
PIN 17          = !cas3;
PIN 18          = !dtack;
PIN 19          = !ras;



/**     Logic Equations **/

!ras            = !c3 & cdac # !c3 & c1;

mux             = c3 & cdac & dtack
                      # mux & !c1
                      # mux & cdac;

!cas0           = (!cas0 & cdac # !c1) & !(ram_sel & !a19 & !a20)
                      # !c1 & !mux
                      # !cas0 & c1 & ram_sel & !a19 & !a20;

!cas1           = (!cas1 & cdac # !c1) & !(ram_sel & a19 & !a20)
                      # !c1 & !mux
                      # !cas1 & c1 & ram_sel & a19 & !a20;
```

```
!cas2           = (!cas2 & cdac # !c1) & !(ram_sel & !a19 & a20)
                        # !c1 & !mux
                        # !cas2 & c1 & ram_sel & !a19 & a20;

!cas3           = (!cas3 & cdac # !c1) & !(ram_sel & a19 & a20)
                        # !c1 & !mux
                        # !cas3 & c1 & ram_sel & a19 & a20;

dtack           = !dtack & c3 & (!cas0 # !cas1 # !cas2 # !cas3)
                        & c1 & !cdac & ram_sel # dtack & ram_sel;

a17muxa18       = a17 & cdac & ram_sel
                        # a18 & !cdac & ram_sel;
```